Electronic Version
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Claims

[c1] A method for fabricating a vertical semiconductor structure, the method comprising the steps of:
providing a semiconductor substrate comprising a semiconductor material;
forming a deep trench in the semiconductor substrate;
depositing a first gate dielectric layer on a side wall of the deep trench;
filling the deep trench with a filling material;
forming a first source/drain region and a second source/drain region around and along the depth of the deep trench;
forming first and second shallow trench isolation regions sandwiching the deep trench in an active region, the first and second shallow trench isolation regions abutting the active region via first and second abutting surfaces, respectively, wherein the first and second abutting surfaces are parallel to each other and are perpendicular to an orientation plane of the semiconductor material of the substrate;
removing the first gate dielectric layer so as to expose the semiconductor material in the deep trench to the atmosphere;

chemically etching the exposed semiconductor material in the deep trench;
depositing a second gate dielectric layer on a side wall of the deep trench; and
forming a gate terminal for the vertical semiconductor structure in the deep trench.

[c2] The method of claim 1, wherein a top surface of the substrate is perpendicular to the orientation plane of the semiconductor material of the substrate.

[c3] The method of claim 1, wherein the step of filling the deep trench comprises the steps of:
forming a storage node at a bottom of the deep trench; and
forming a trench top oxide layer over the storage node in the deep trench,
wherein the first source/drain region is at a top of the substrate and the second source/drain region is at about the level of the trench top oxide layer.

[c4] The method of claim 3, wherein the storage node being in physical contact with the semiconductor material outside the deep trench such that thermal diffusion of dopants from the storage node forms the second source/drain region.

[c5] The method of claim 3, further comprising the step of forming a collar oxide around the storage node so as to reduce the vertical leakage current from the second source/drain region along with side wall of the deep trench when the storage node is charged positively.

[c6] The method of claim 3, wherein the trench top oxide layer is thicker than the first gate dielectric layer.

[c7] The method of claim 1, wherein the step of filling the deep trench comprises the step of forming a dielectric spacer at the top of the deep trench.

[c8] The method of claim 1, wherein the step of removing the first gate dielectric layer so as to expose the semiconductor material in the deep trench to the atmosphere comprises the steps of:
removing the filling material from the deep trench until the first gate dielectric layer is exposed to the atmosphere; and
etching the first gate dielectric layer until the semiconductor material is exposed to the atmosphere in the deep trench.

[c9] The method of claim 1, wherein the step of chemically etching the exposed semiconductor material in the deep trench is performed until the exposed semiconductor

material recesses to a plane parallel to the orientation plane.

[c10] The method of claim 1, wherein the step of chemically etching the exposed semiconductor material in the deep trench comprises the step of etching with ammonia hydroxide.

[c11] A vertical semiconductor structure, comprising:
first and second shallow trench isolation regions formed in a substrate comprising a semiconductor material; and
a first vertical transistor formed in the substrate and sandwiched between the first and second shallow trench isolation regions, the first vertical transistor including first and second source/drain regions, a first channel region, a gate region, and a first gate dielectric layer sandwiched between the gate region and the first channel region,
wherein the first channel region abuts the first and second shallow trench isolation regions via first and second abutting surfaces, respectively, and
wherein the first and second abutting surfaces are perpendicular to an orientation plane of the semiconductor material of the substrate.

[c12] The structure of claim 11, wherein the first gate dielectric layer abuts the first channel region via a third abut-

ting surface, wherein the third abutting surface is parallel to the orientation plane.

[c13] The structure of claim 12, wherein a top surface of the substrate is perpendicular to the orientation plane.

[c14] The structure of claim 12, further comprising
a second vertical transistor formed in the substrate and sandwiched between the first and second shallow trench isolation regions, the second vertical transistor including third and fourth source/drain regions, a second channel region, the gate region, and a second gate dielectric layer sandwiched between the gate region and the second channel region,
wherein the second channel region abuts the third and fourth shallow trench isolation regions via fourth and fifth abutting surfaces, respectively, and
wherein the third and fourth abutting surfaces are perpendicular to the orientation plane of the semiconductor material of the substrate.

[c15] The structure of claim 14, wherein the second gate dielectric layer abuts the second channel region via a sixth abutting surface, wherein the sixth abutting surface is parallel to the orientation plane.

[c16] The structure of claim 14, wherein the first and second

vertical transistors are formed around and along the depth of a deep trench.

[c17] The structure of claim 14, wherein a top surface of the substrate is perpendicular to the orientation plane.

[c18] A method for fabricating a vertical semiconductor structure, the method comprising the steps of:
providing a semiconductor substrate comprising a semiconductor material;
forming a deep trench in the semiconductor substrate;
depositing a first gate dielectric layer on a wall of the deep trench;
filling the deep trench with a filling material and recessing the filling material in the deep trench down to a recess depth;
removing the first gate dielectric layer on a side wall of the deep trench down to a level lower than the recess depth;
filing the deep trench with poly silicon and recessing the poly silicon down to a level above the recess depth;
filling the deep trench with a second dielectric layer and selectively removing the dielectric on a wall of the deep trench so as to form a trench top dielectric layer;
filling the deep trench with poly silicon;
forming a first source/drain region and a second source/drain region around and along the depth of the deep

trench;

forming first and second shallow trench isolation regions sandwiching the deep trench in an active region, the first and second shallow trench isolation regions abutting the active region via first and second abutting surfaces, respectively, wherein the first and second abutting surfaces are parallel to each other and are perpendicular to an orientation plane of the semiconductor material of the substrate;

removing the first gate dielectric layer so as to expose the semiconductor material in the deep trench to the atmosphere;

chemically etching the exposed semiconductor material in the deep trench;

depositing a second gate dielectric layer on a side wall of the deep trench; and

forming a gate terminal for the vertical semiconductor structure in the deep trench.

[c19] The method of claim 18, wherein a top surface of the substrate is perpendicular to the orientation plane.

[c20] The method of claim 18, wherein the step of chemically etching the exposed semiconductor material in the deep trench comprises the step of etching with ammonia hydroxide.